



The BNL Silicon Multi-element detector system for dilute EXAFS experiments

D. Peter Siddons, Anthony J. Kuczewski

National Synchrotron Light Source, Brookhaven National Laboratory, Upton, NY

Gianluigi De Geronimo, Paul O'Connor

Microelectronics Group, Instrumentation Division, Brookhaven National Laboratory, Upton, NY

Rolf H. Beuttenmuller, Zheng Li

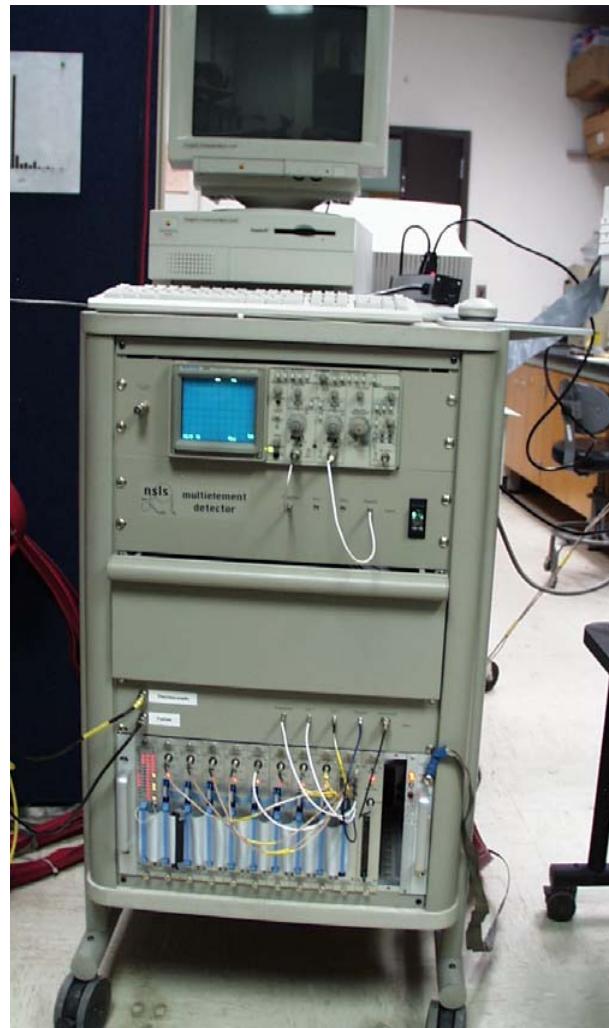
Semiconductor Lab., Instrumentation Division, Brookhaven National Laboratory, Upton, NY

Current EXAFS detector



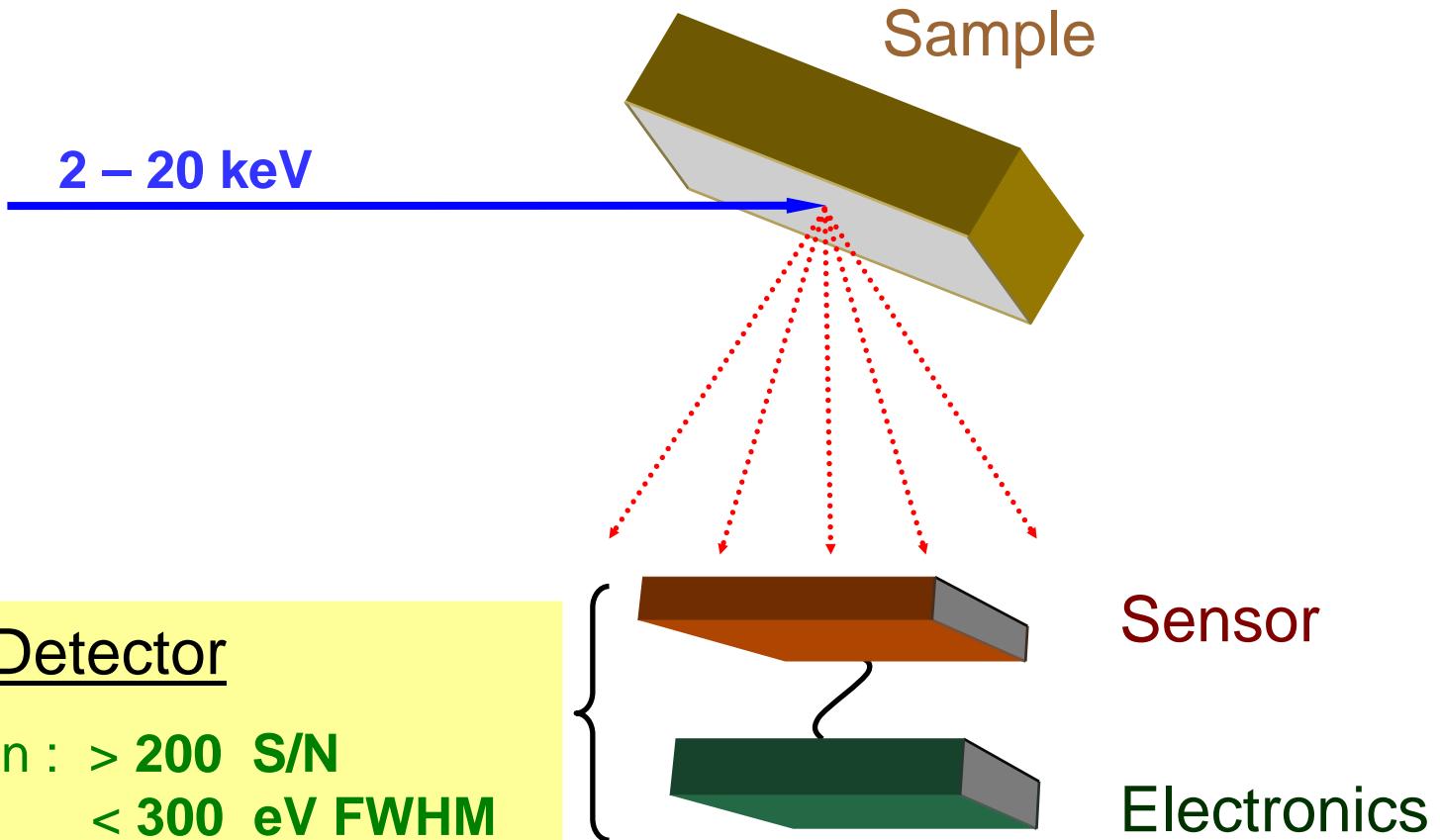
head - preamplifiers

≈ 100 channels, > 350 eV, < 1 MHz



rack – shapers ...

Typical fluorescence EXAFS spectroscopy geometry



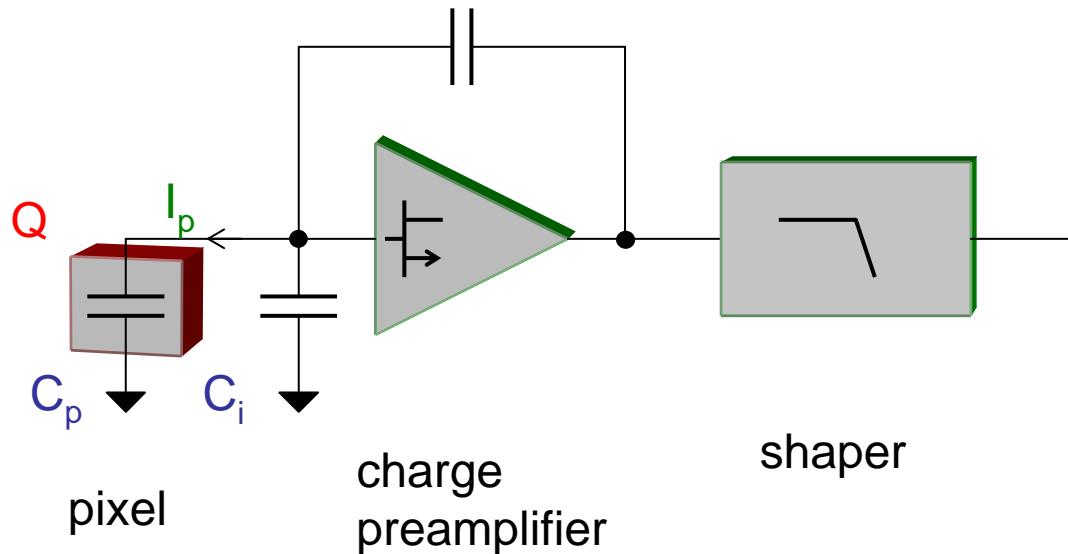
Detector

- Resolution : > 200 S/N
< 300 eV FWHM
- Rate : > 10 MHz/cm²
> 100 kHz/pixel
- Spectroscopy (energy windows)

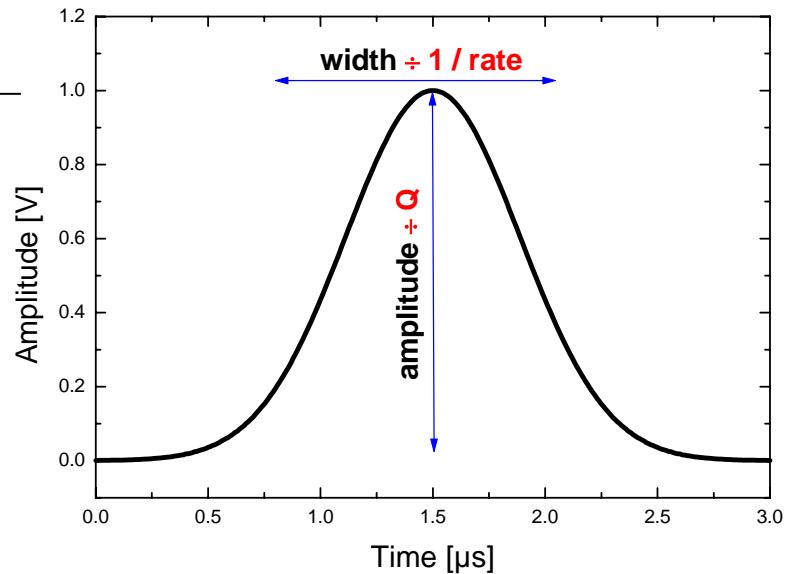
Sensor

- front-end
- processing
- readout

Resolution vs Rate

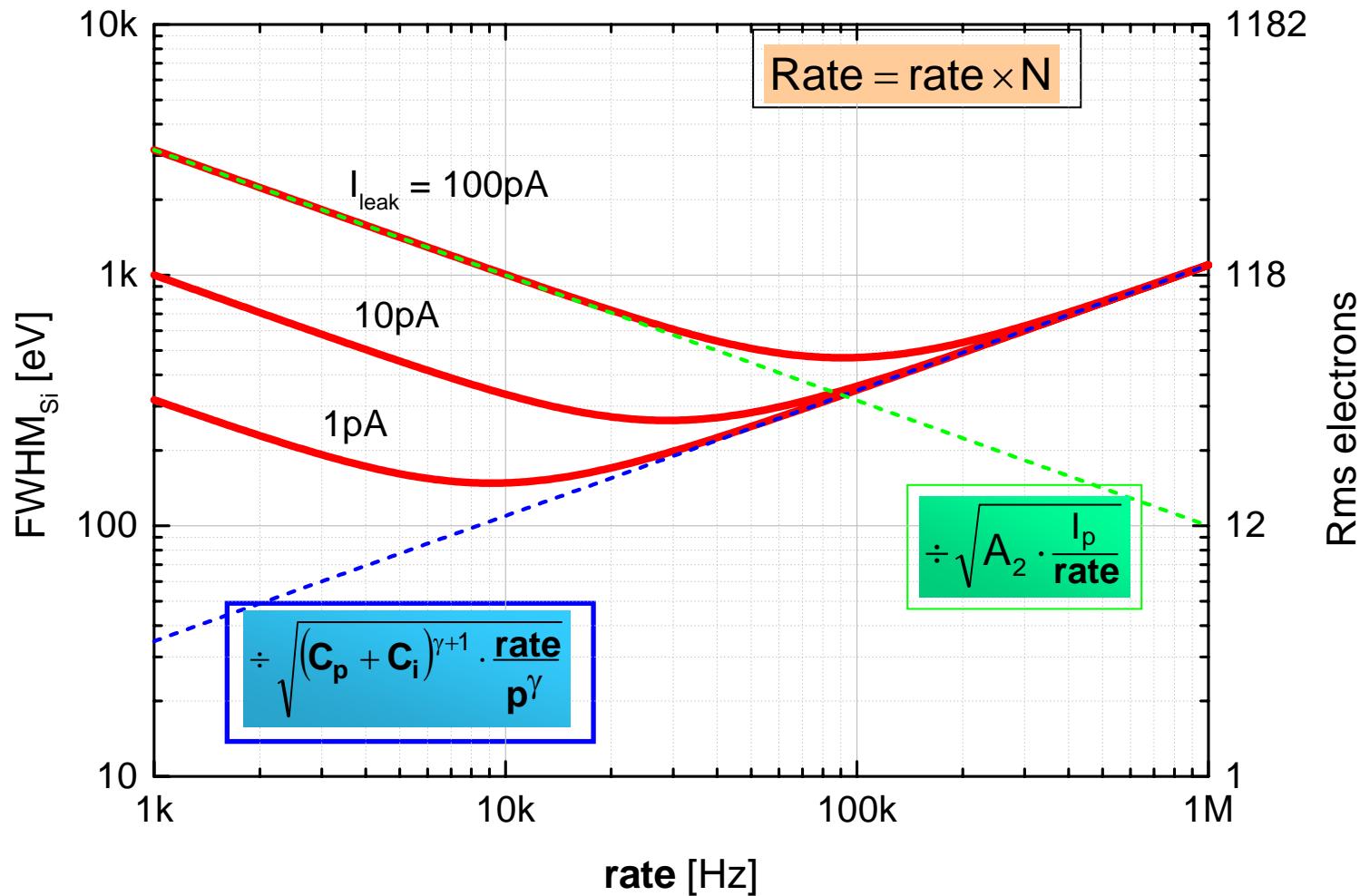


$$\text{rate} = \frac{\text{Rate}}{N} \quad (N = \text{number of pixels})$$

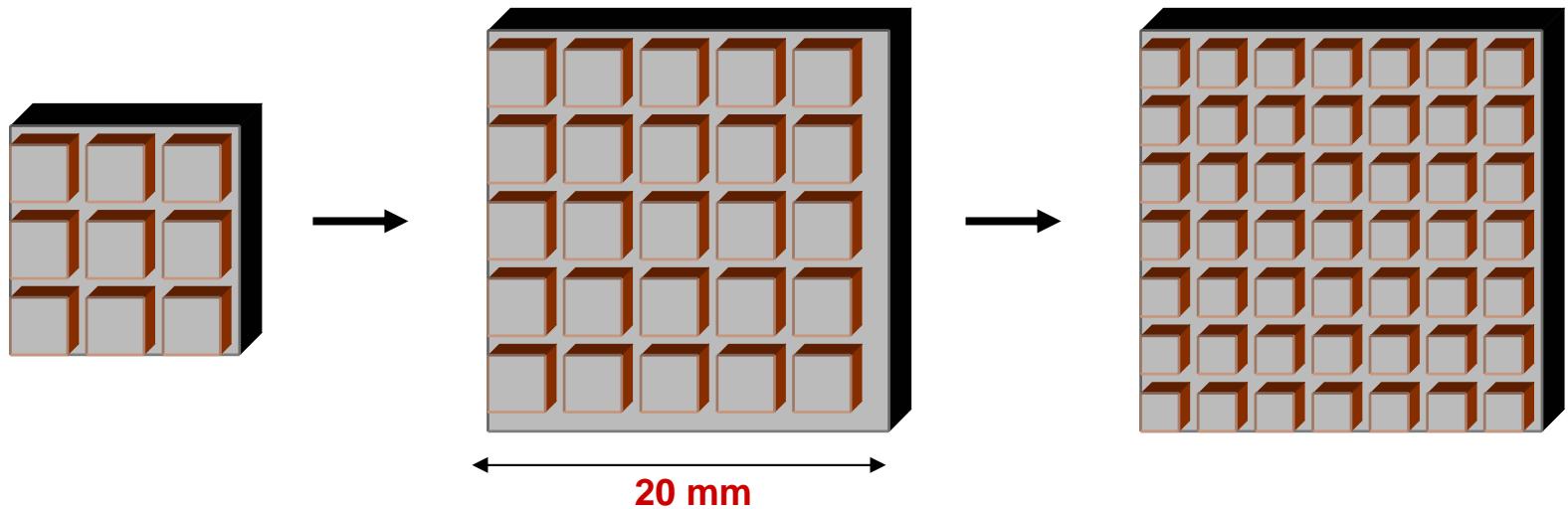


$$\text{ENC}^2 = A_1(\gamma) (C_p + C_i)^{\gamma+1} \frac{\text{rate}}{p^\gamma} + A_2 \frac{I_p}{\text{rate}} \quad 0 < \gamma < 1$$

Resolution vs Rate



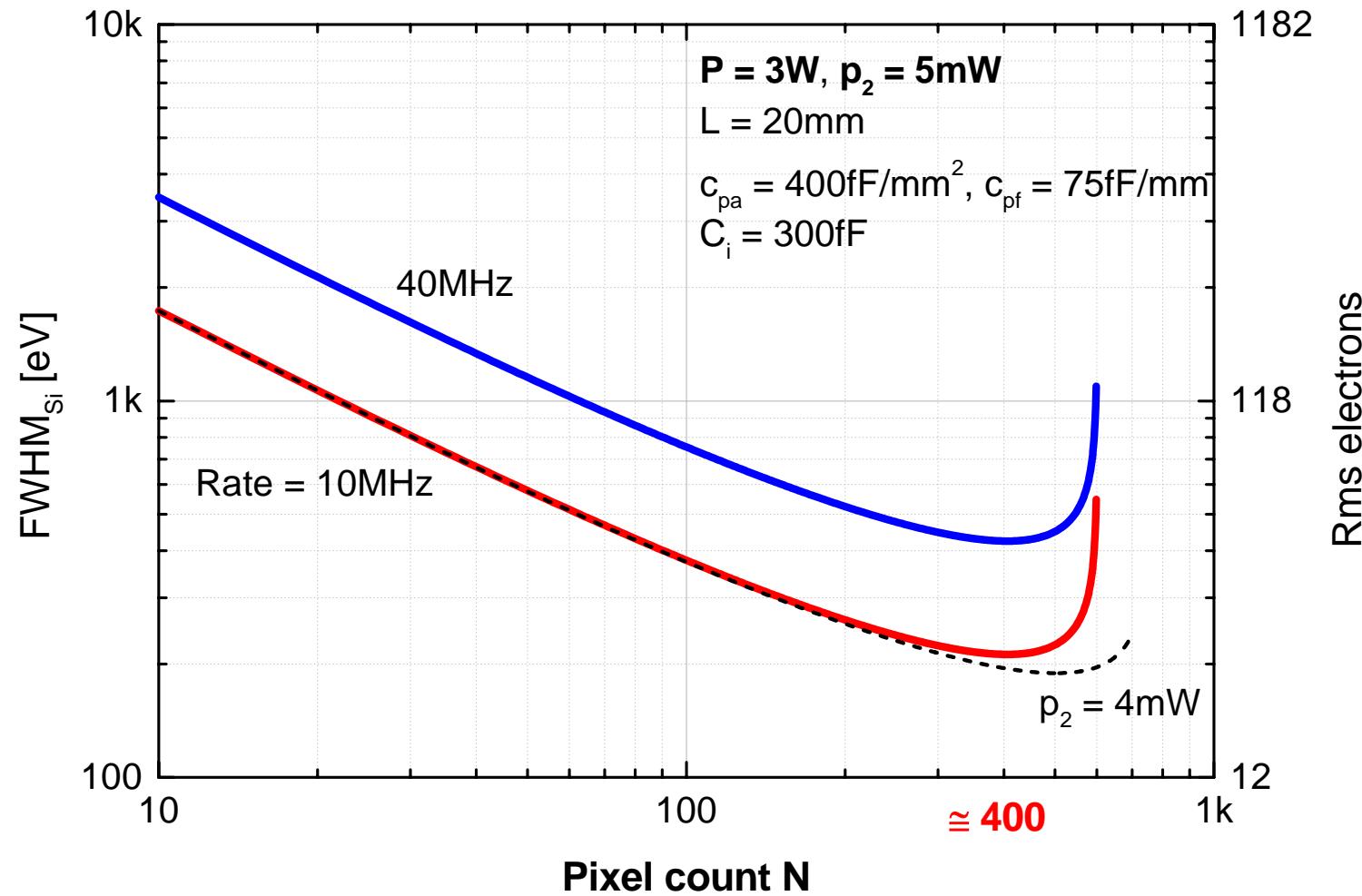
Optimum pixellation

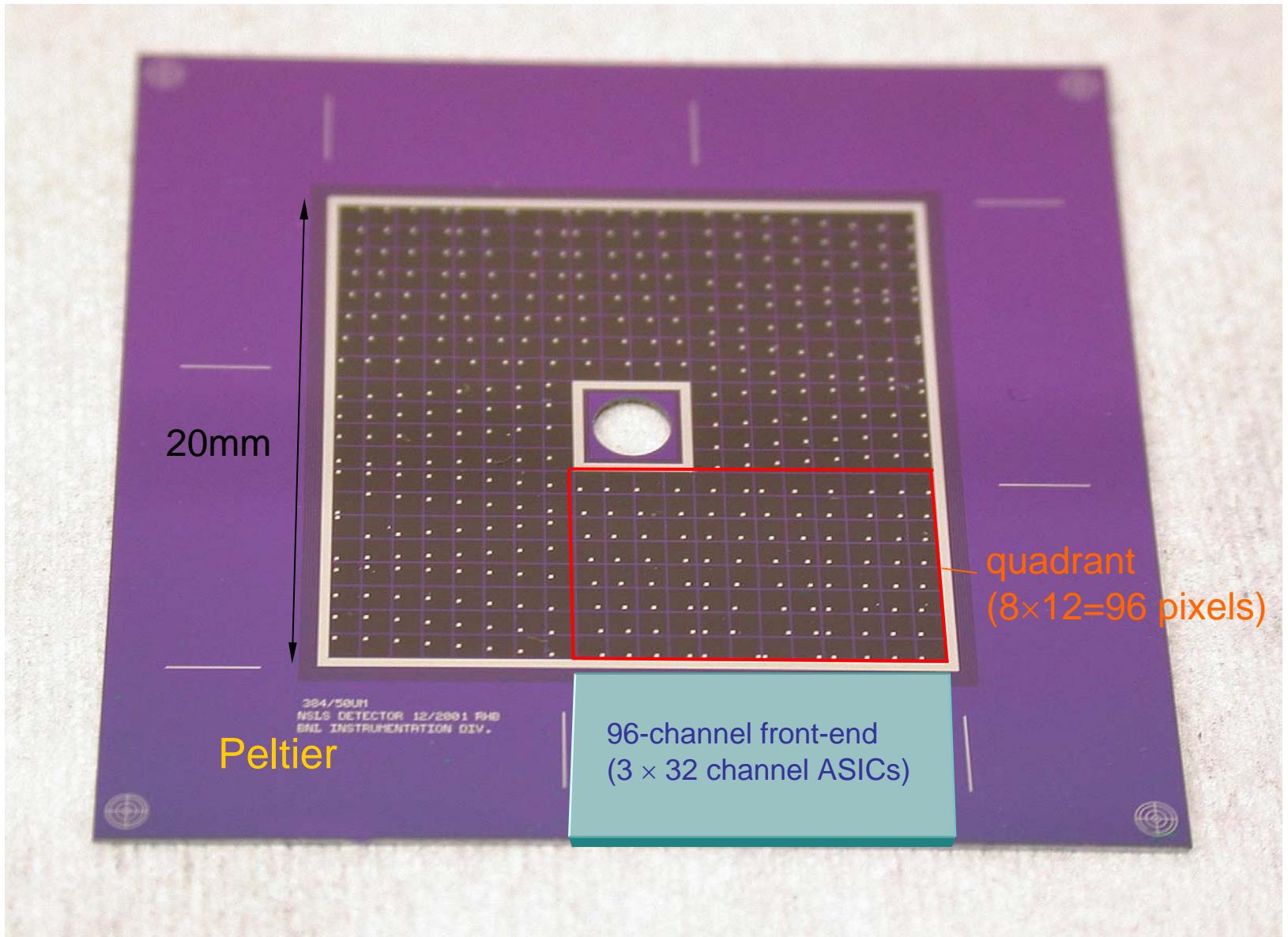


$$\text{ENC}^2 \div (C_p(N) + C_i)^{\gamma+1} \frac{\text{Rate}}{\left(\frac{P}{N} - p_2\right)^\gamma}$$

- charge sharing ($\approx 20\mu\text{m}/\text{side}$) and trapping (gap/ side) : empirical

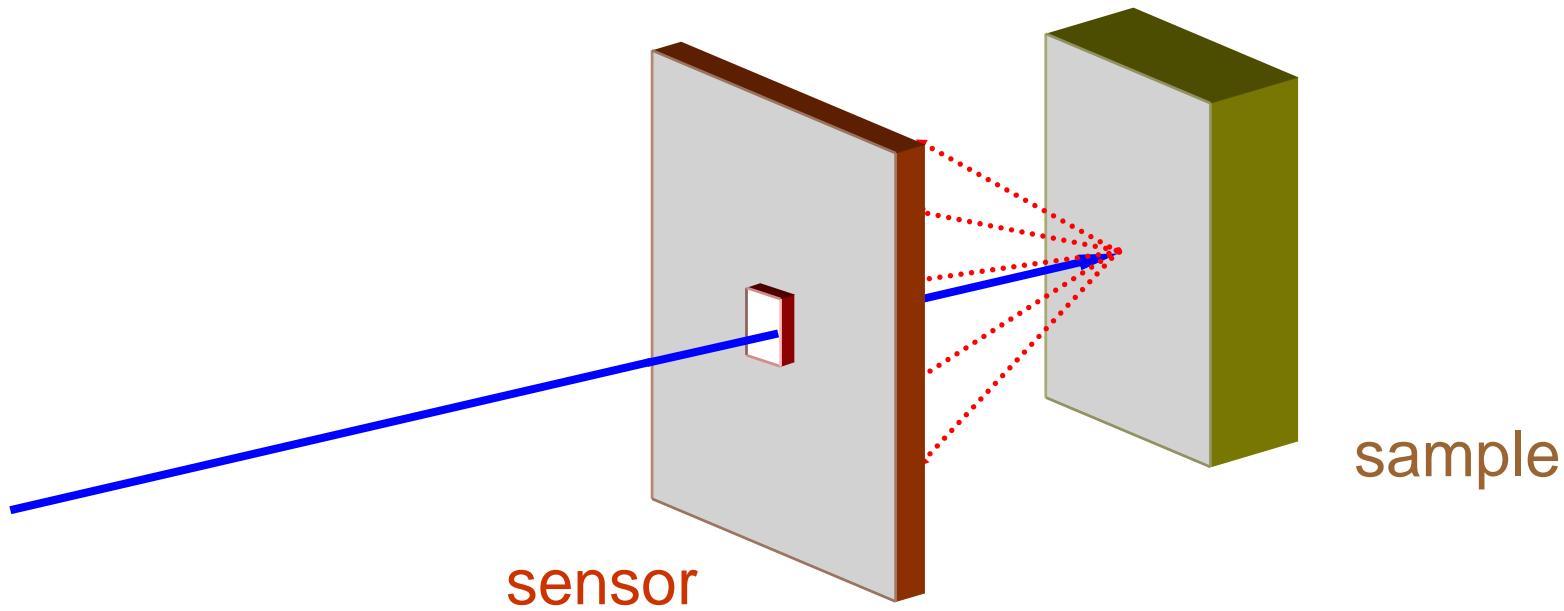
Optimum pixellation



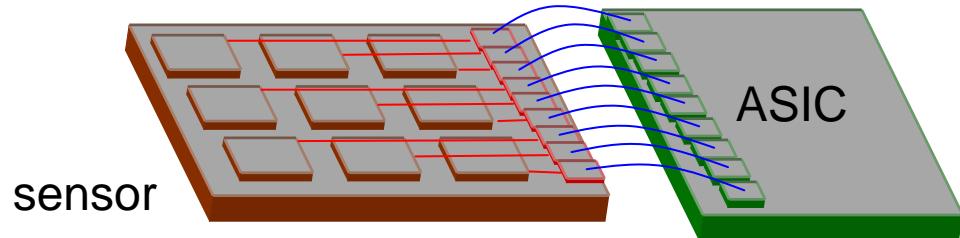
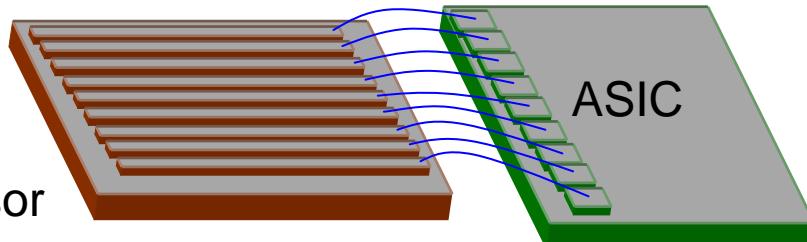


Si n-type high resistivity wafer 250 μ m thick,
N = 384 p⁺ \approx 1mm \times 1mm pixels, C_p \approx 700-1000fF
gaps 10 μ m, 30 μ m, 50 μ m

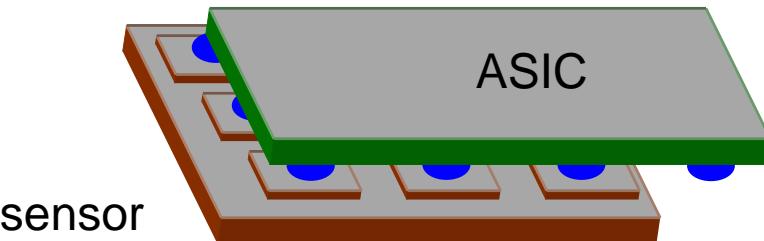
Beam through



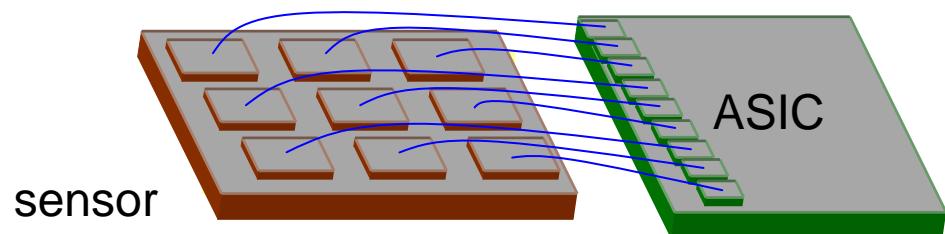
Interconnecting pixel to front-end electronics



- + interconnect parasitic
- + bond length
- fringe capacitance
- charge sharing and trapping



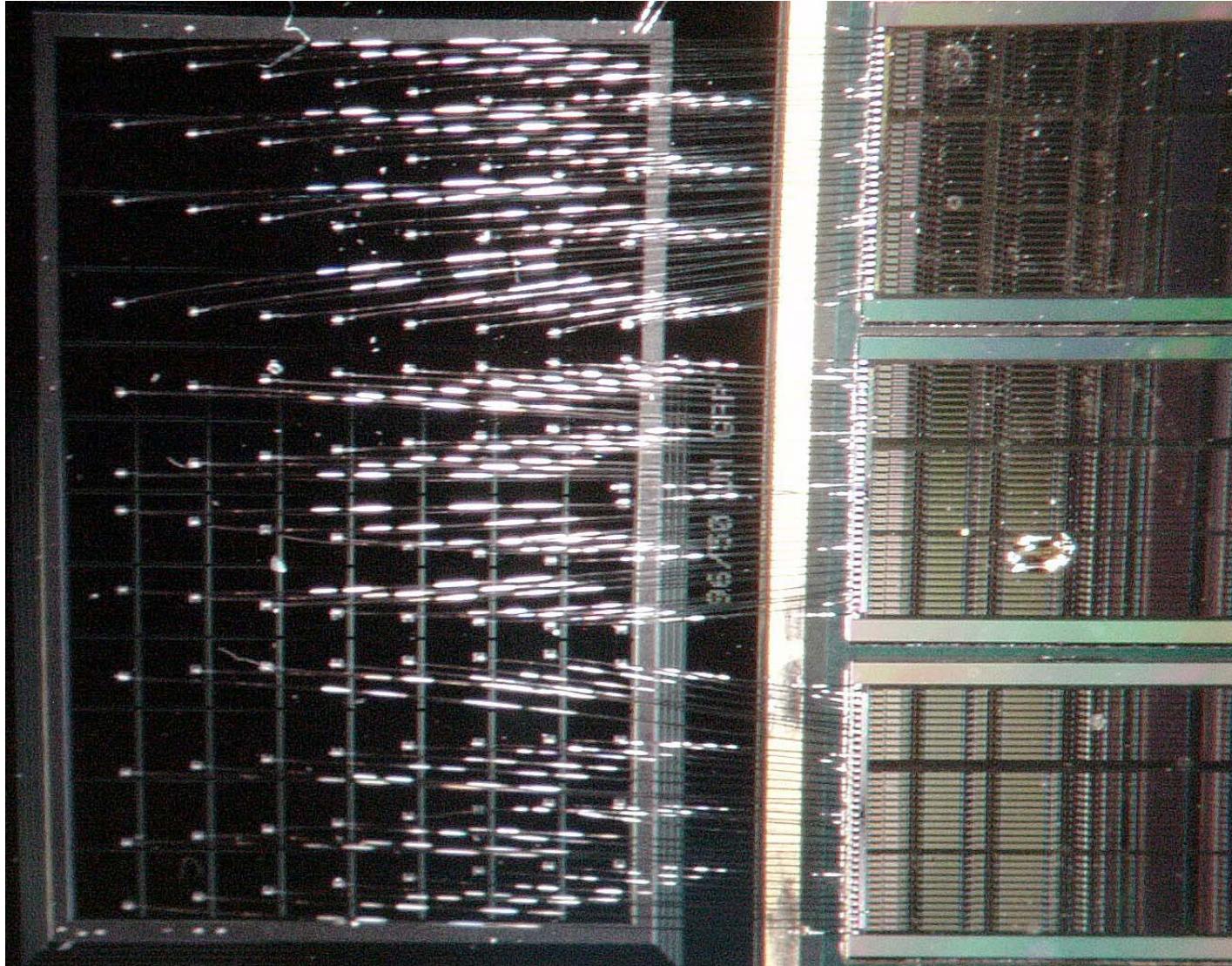
- + interconnect parasitic
- constraint on ASIC area and layout
- fluorescence from Pb (Sn/Pb/Ag)
- illumination from segmented side



- + dielectric losses
- ± interconnect parasitic
- bond length

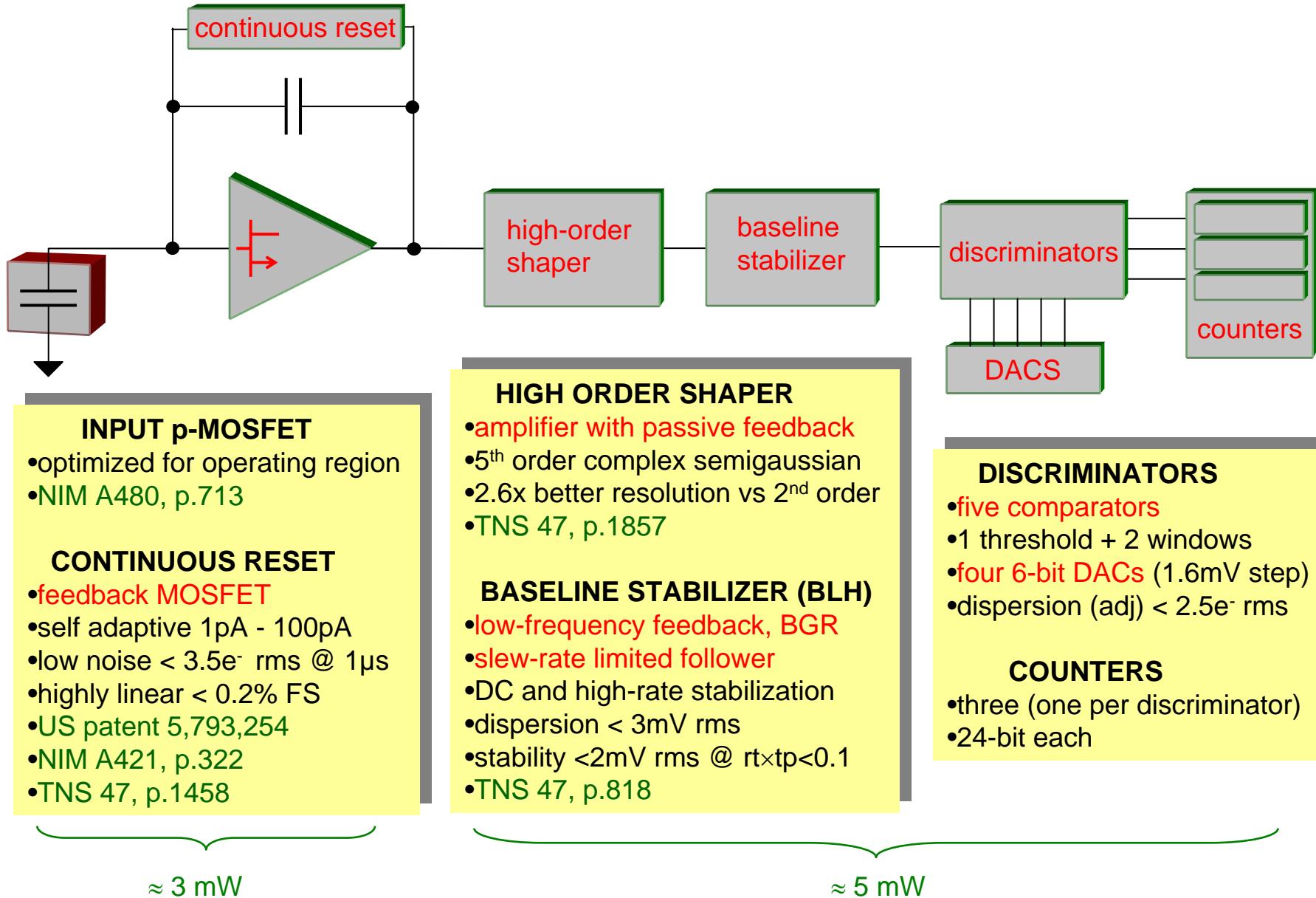
$$6\text{mm} \times 10\mu\text{m}, \text{Si}_3\text{N}_4 (\epsilon_r=6.5, \tan(\delta) \approx 1\text{m}), 3\mu\text{m}, \delta C_i \approx 1.2\text{pF}$$
$$\delta FWHM_{loss} = 8.5/q \cdot \sqrt{(2kTC_i \tan(\delta))} \approx 180\text{eV}$$

Sensor – ASIC photo

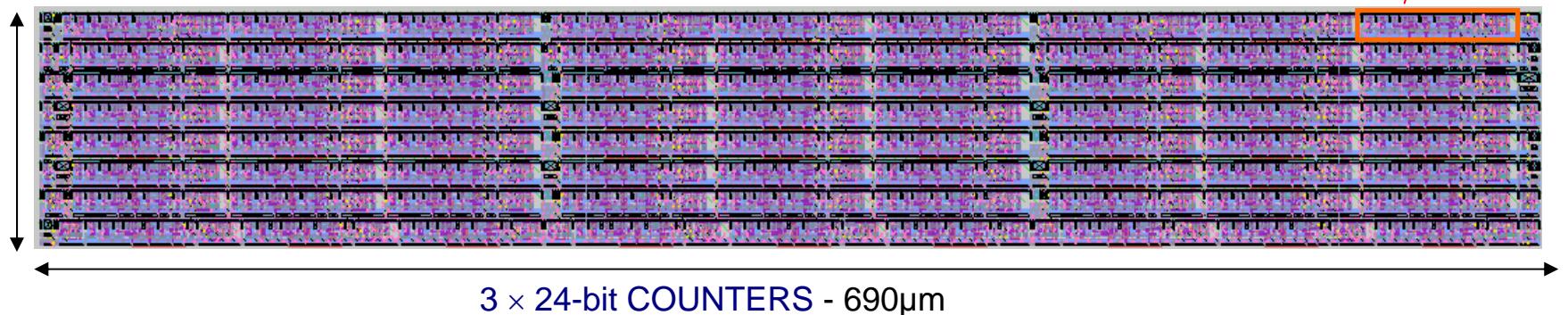
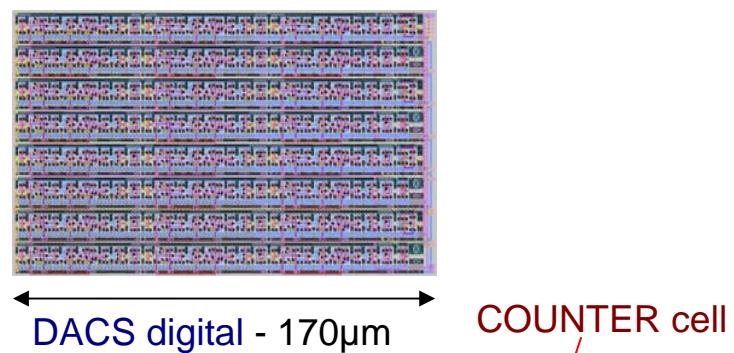
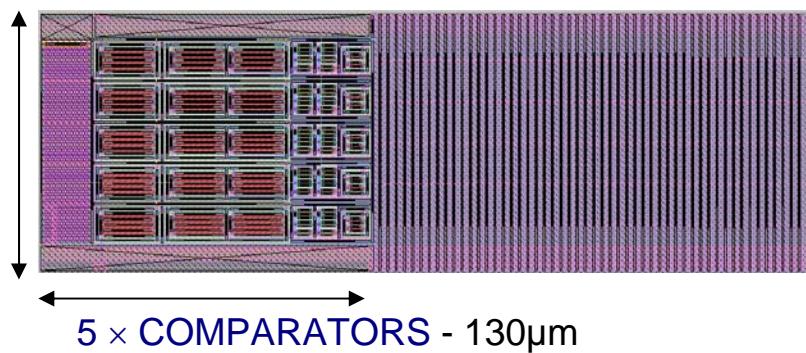
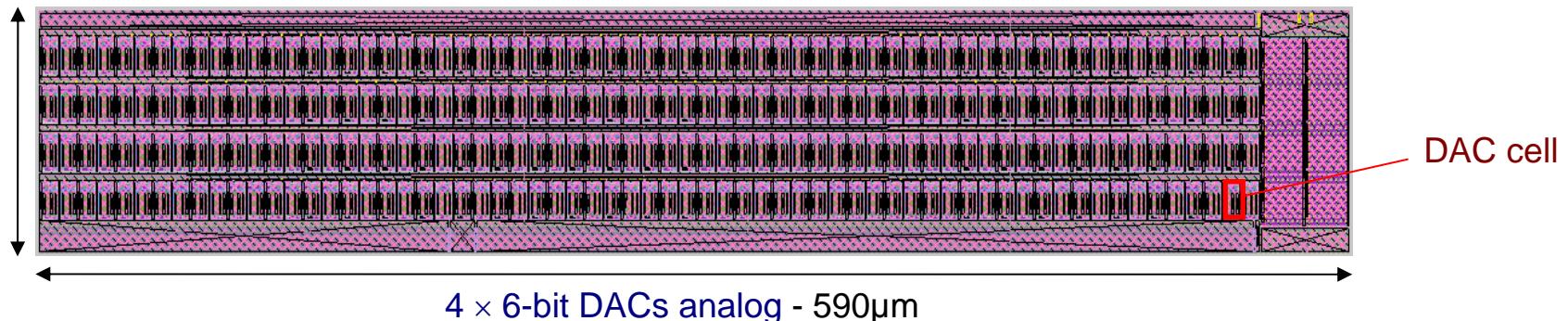


one quadrant

ASIC channel overview



ASIC layout cells



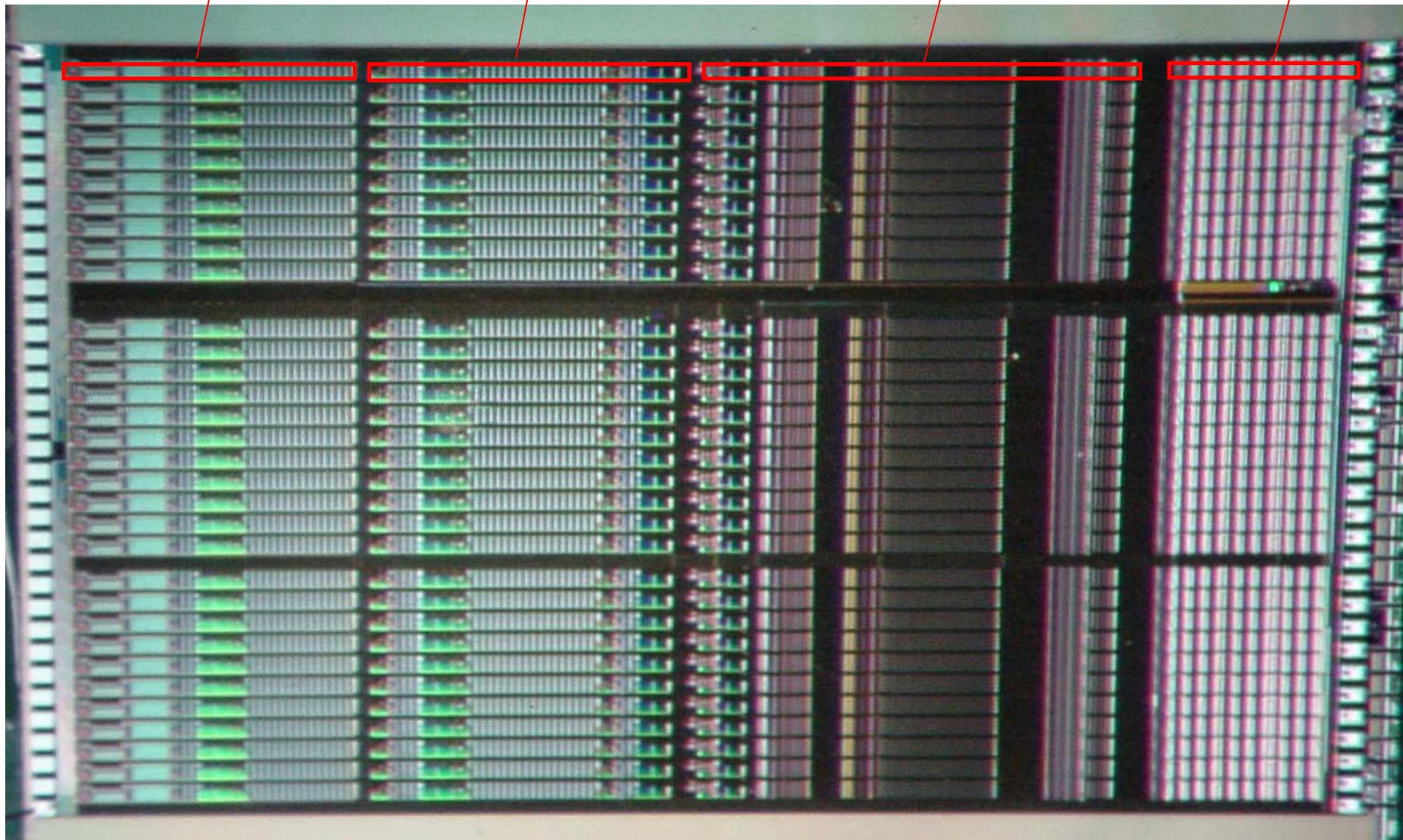
ASIC photo

charge preamplifier

shaper with BLH

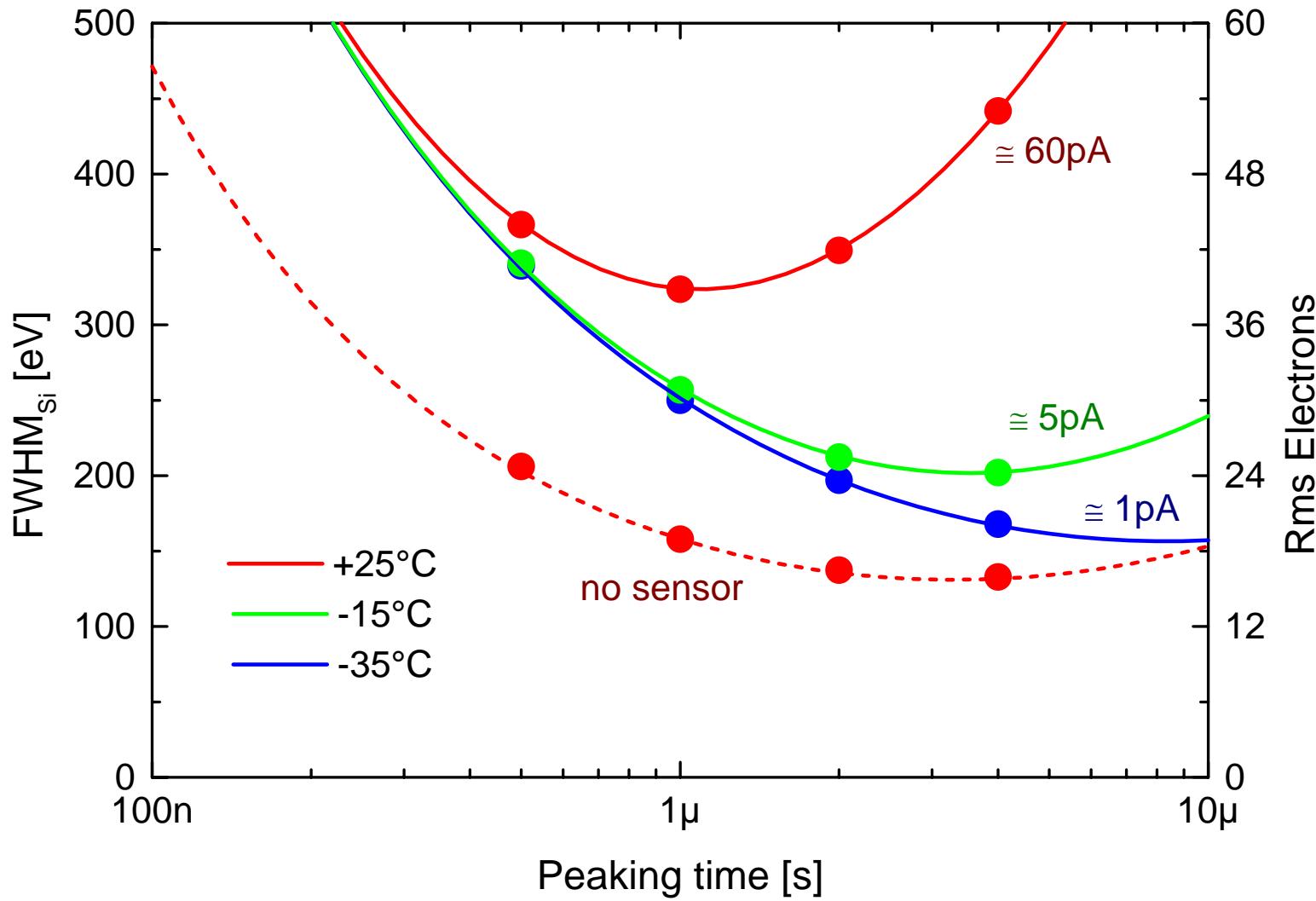
discriminators and DACs

counters



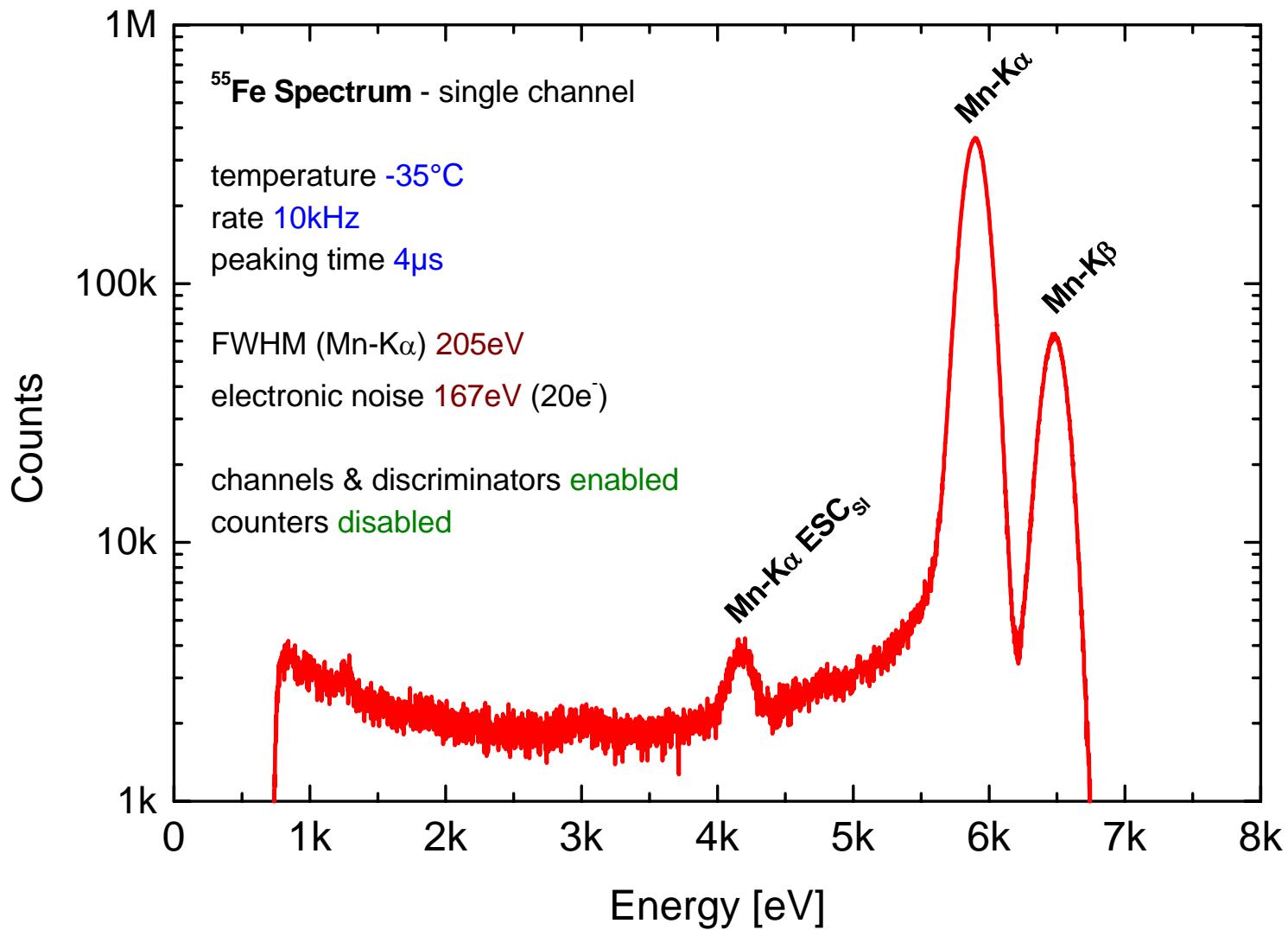
32 channels, $3.6 \times 6.3 \text{ mm}^2$

Measured resolution



50 μm -gap, $C_p \approx 700\text{fF}$, $C_{\text{i-bond}} \approx 50\text{-}200\text{fF}$, $C_{\text{i-pad}} \approx 220\text{fF}$

^{55}Fe spectrum



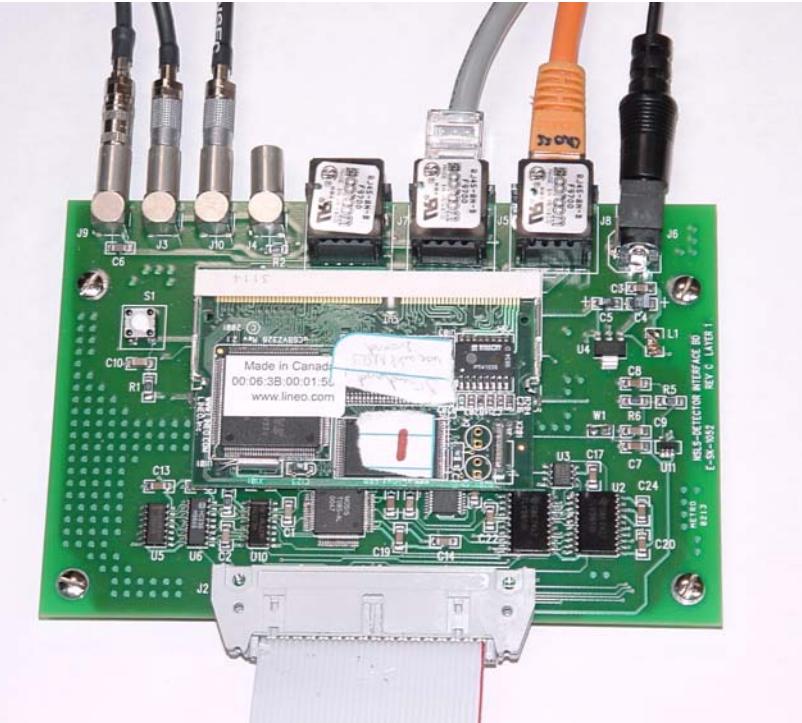
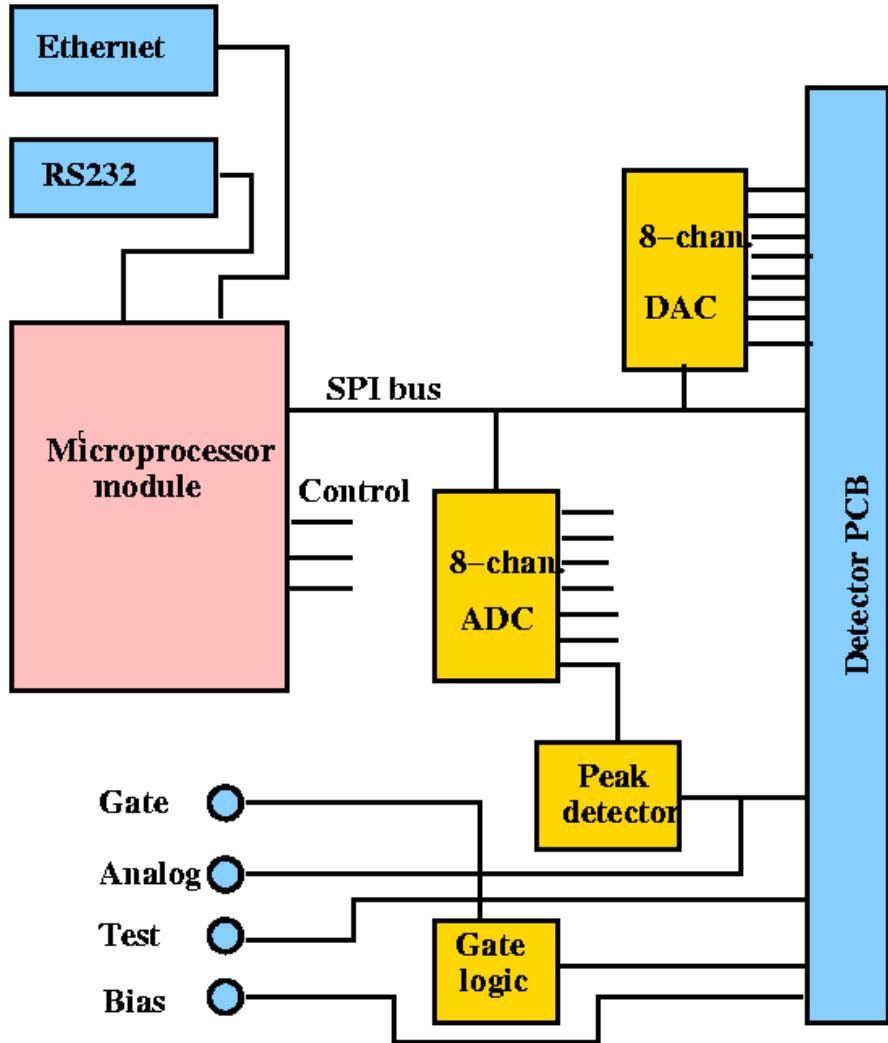
50 μm -gap, $C_p \approx 700\text{fF}$, $C_{\text{i-bond}} \approx 50\text{-}200\text{fF}$, $C_{\text{i-pad}} \approx 220\text{fF}$

ASIC overview

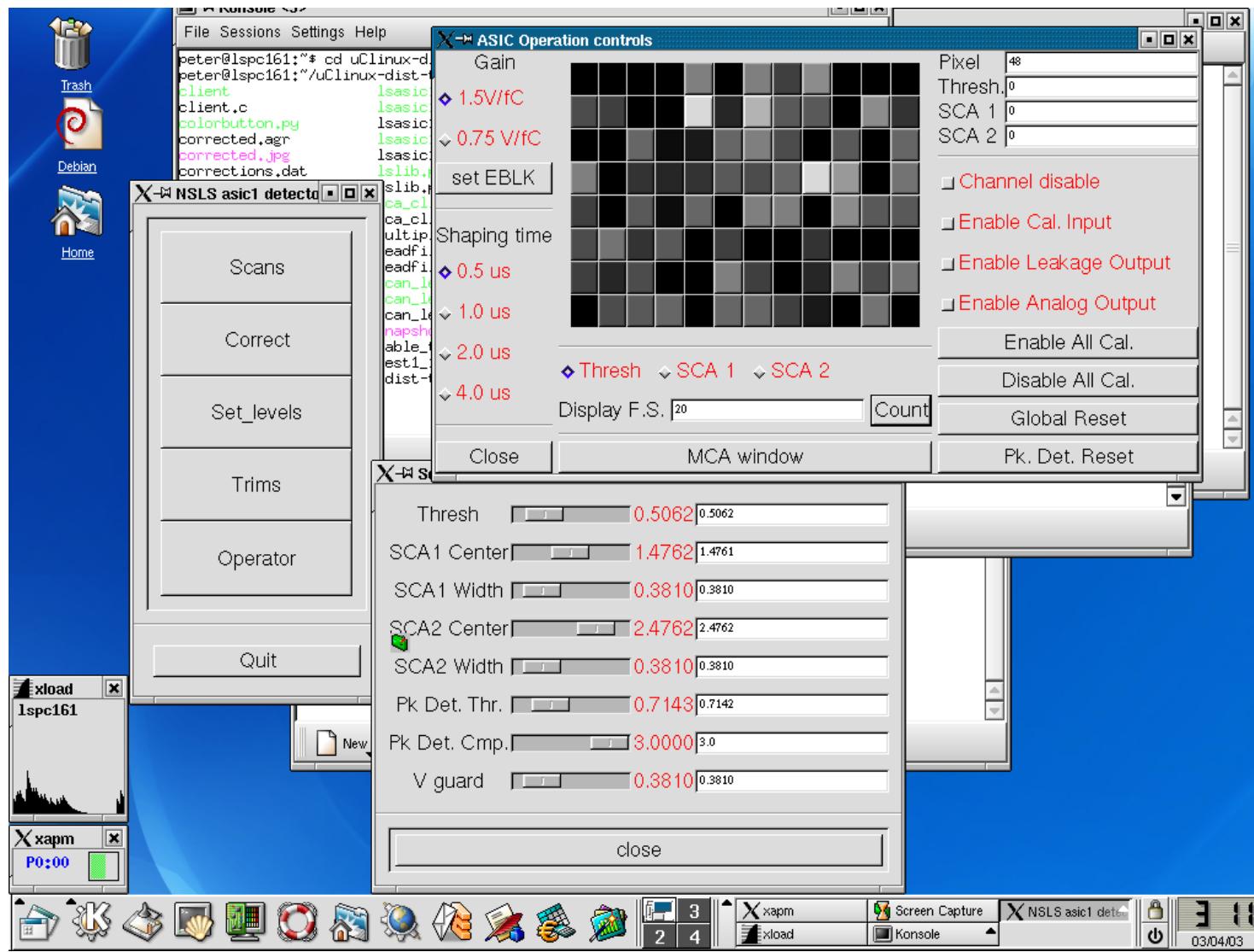
Technology	CMOS 0.35μm 3.3V 2P4M
Size	$\approx 3.6 \times 6.3 \text{ mm}^2$
# MOSFETs	$\approx 180,000$
# Channels	32
power / channel	$\approx 8 \text{ mW}$
# Discriminators	three / channel (1 thr., 2 win.)
threshold adjustment	four 6-bit DACs (1.6mV step)
threshold dispersion (adj)	$\approx 2.5 \text{ electrons rms}$
# Counters	three / channel
bits per counter	24
Gain (settable)	750, 1500 mV/fC
Peaking time (settable)	0.5, 1, 2, 4 μs
ENC @ 1μs	$\approx 14 + 12/\text{pF}$ electrons rms
ENC @ 4μs	$\approx 11 + 6/\text{pF}$ electrons rms

- self adaptive continuous **reset**
- high order **shaper**
- **band-gap** referenced output baseline
- output baseline **stabilizer** (BLH)
- **test** capacitors
- analog and pixel leakage monitors
- plug & play (fully self biasing)
- serial interface
 - counters readout
 - gain / peaking-time setting
 - monitors & test enable
 - channel masking
 - DACs setting
- token or chip-select mode

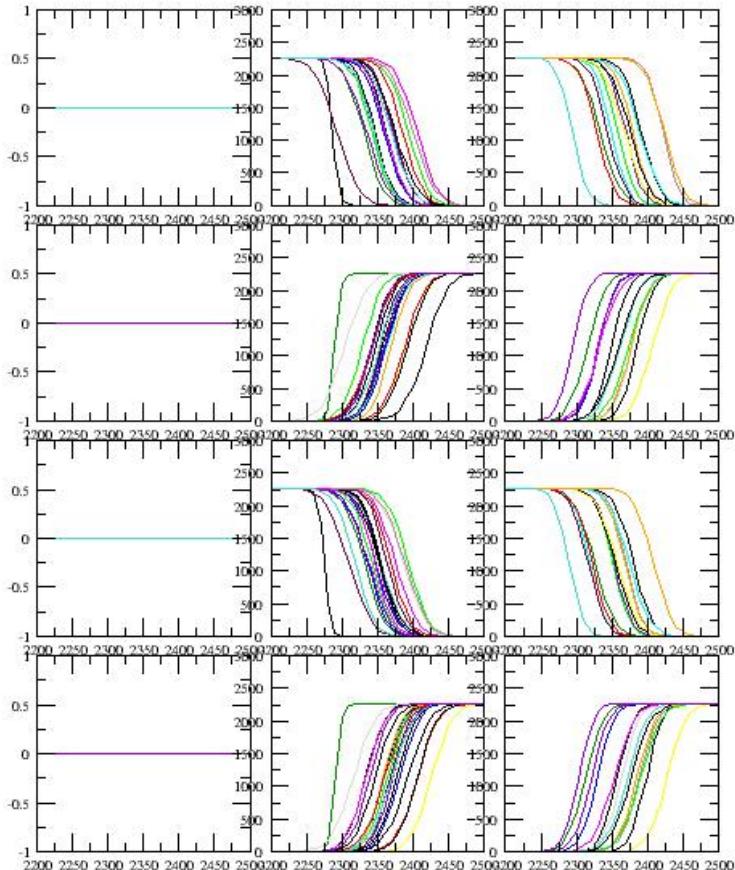
Readout



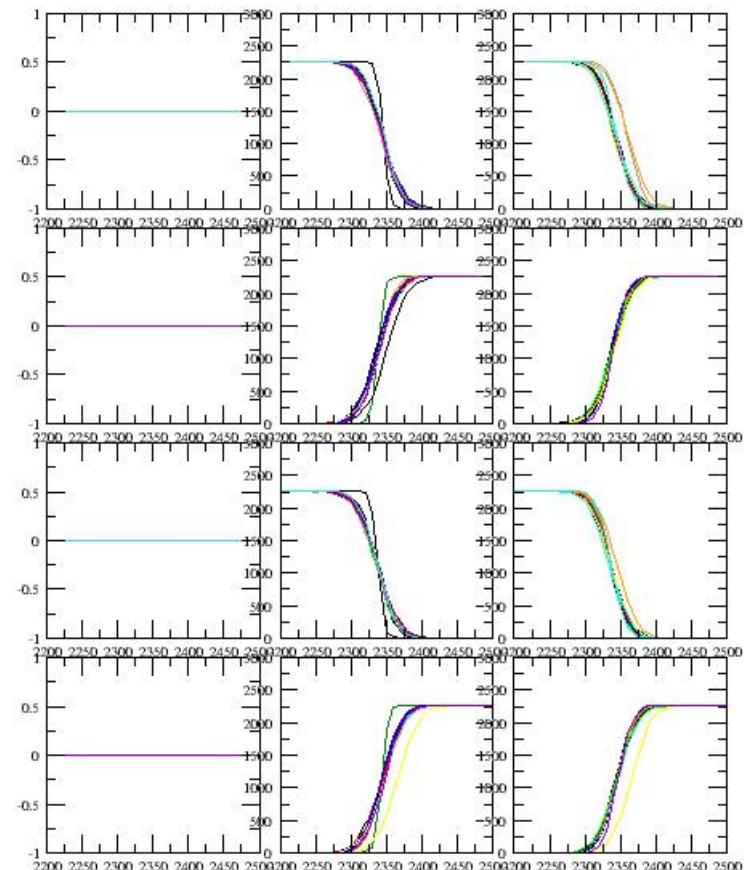
Readout interface



Automatic threshold equalization

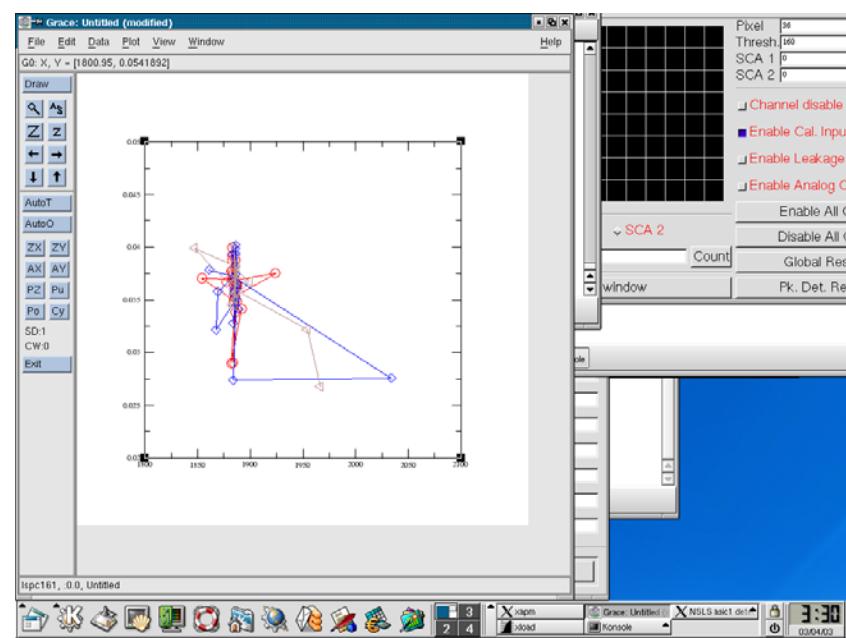
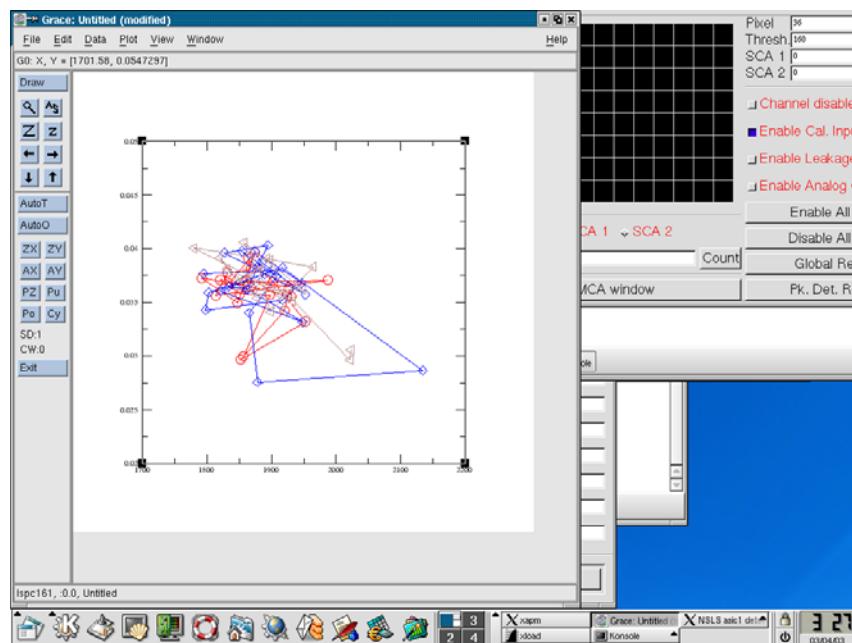


before correction $\sigma \approx 170e^- rms$



after correction $\sigma \approx 2.5e^- rms$

Correction map



Current EXAFS detector



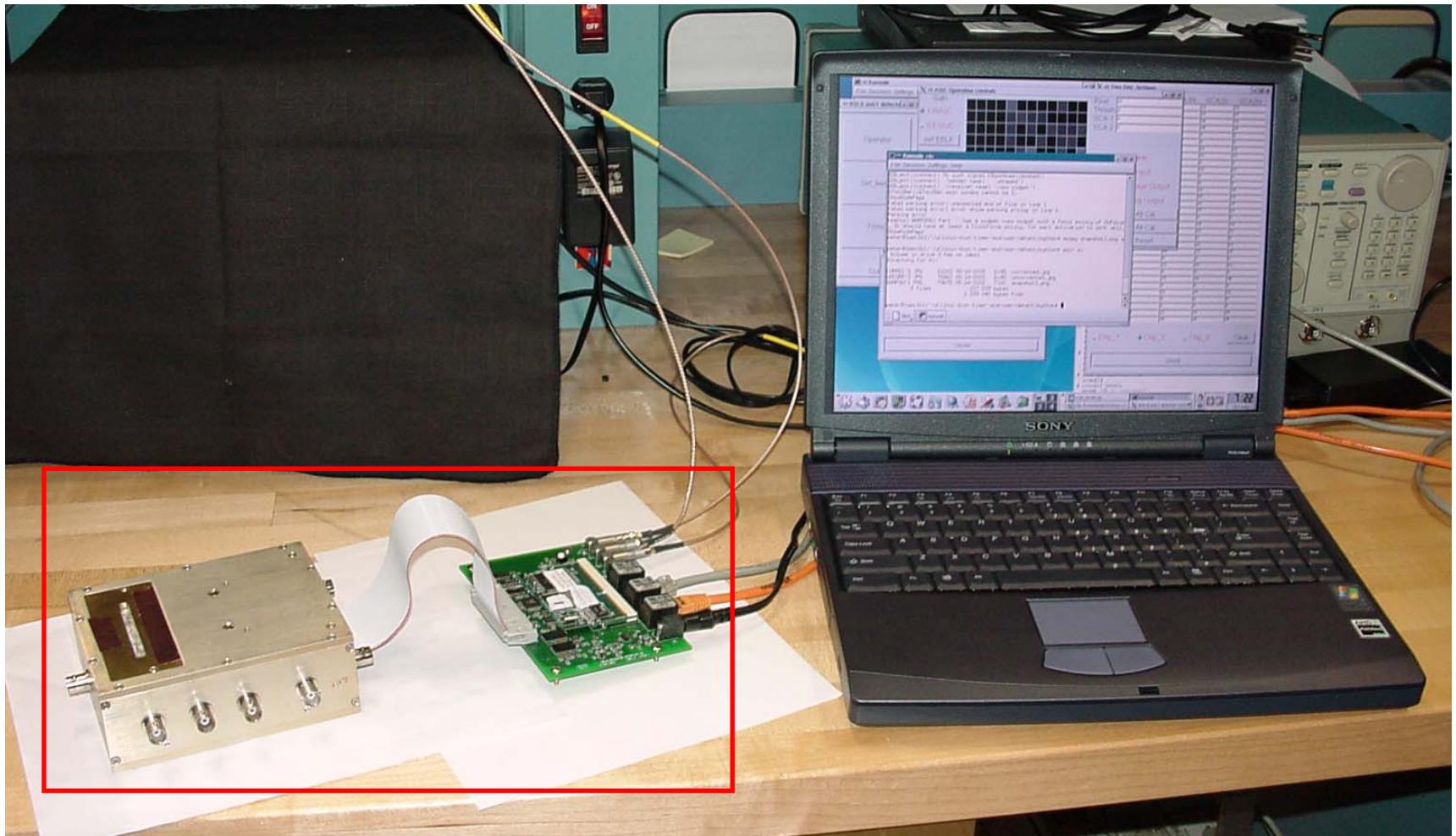
head - preamplifiers

≈ 100 channels, > 350 eV, < 1 MHz



rack – shapers ...

New EXAFS detector



≈ 400 channels, < 300 eV, > 10MHz

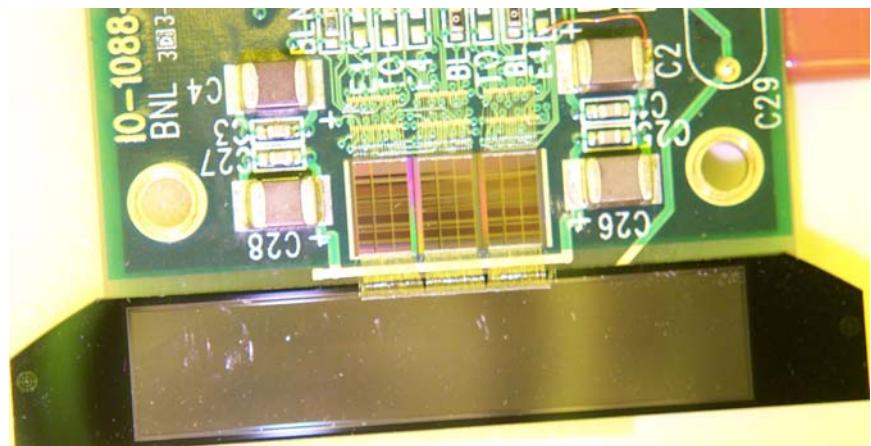
Problems with first ASIC run (and solutions)

- Significant # of channels don't work (~30%)
 - Due to process problem. MOSIS solved.
- Switching any control bit causes whole chip to be disabled for ~3 sec.
 - SPI chain was unbuffered on chip, so all channels were disabled then re-enabled. Re-enable needs 3 sec. Buffering added
- BLH fails for negative pulses.
 - Any undershoot (e.g. during overload recovery) causes baseline shift for a significant time. Due to asymmetric behavior of BLH. Added symmetry components. Simulations shows problem and suggests fix will be successful.
- Second run due soon. All bugs should be fixed ☺

Silicon strip detector

A detector consisting of 0.125mm strips of length 8mm.

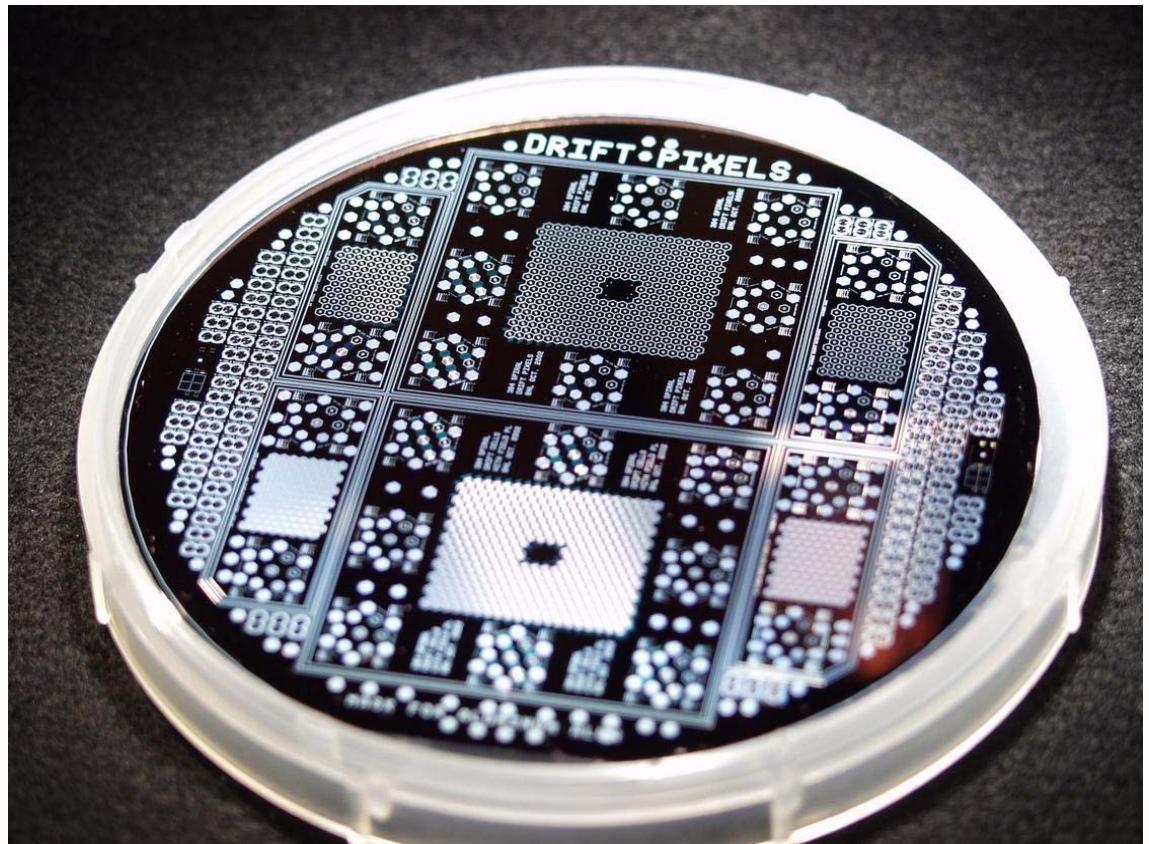
This will be used for diffraction applications or other apps where 1-D position sensitivity is required with good energy resolution.



Drift-Detector Array

Drift-detectors give large area while keeping low capacitance by ‘drifting’ charge through bulk of silicon to a small collector electrode.

Wafer has 96- and 384-element arrays.



Summary

New detector for EXAFS

- monolithic Si sensor, 400-mm² active area
- ≈ 400 1-mm² pixels
- 32-channel ASICs

Future work

- one ASIC iteration
- pixel gap selection (10, 30, 50 μm)
- four quadrant (12 ASICs) assembly / test
- extended user testing at NSLS

First results (single quadrant)

- ENC $\approx 11 + 6/\text{pF e}^- \text{ rms}$ @ 4 μs
- FWHM < 300eV @ rate < 100 kHz/pixel
- threshold dispersion < 2.5 e⁻ rms
- Initial beamline tests: no problems from beamline environment

Next generation

- Per-channel on-chip MCA
 - Microprobes, advanced data processing
- Larger drift-detector arrays